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ENTITLED

WINDOW VIA CAPACITOR

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TITLE: WINDOW VIA CAPACITOR

PRIORITY CLAIMS

This application claims the benefit of U.S. Provisional Application No. 60/415,831, entitled "WINDOW VIA CAPACITOR", filed October 3, 2002 and which is 5 incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

The present subject matter generally concerns improved termination features for multilayer electronic components, 10 and more particularly relates to via connections for multilayer capacitors. Specific formation and arrangement of internal electrode layers with an optional window 15 termination layer facilitates the formation of low-inductance terminations. Such terminations are preferably compatible with ball grid array (BGA) and other device mounting technologies.

Many modern electronic components are packaged as monolithic devices, and may comprise a single component or multiple components within a single chip package. One 20 specific example of such a monolithic device is a multilayer capacitor or capacitor array, and of particular interest with respect to the disclosed technology are multilayer capacitors with interdigitated internal electrode layers and corresponding electrode tabs. Examples of multilayer capacitors that include features of 25 interdigitated capacitor (IDC) technology can be found in

U.S. Patent Nos. 5,880,925 (DuPré et al.) and 6,243,253 B1 (DuPré et al.). Other monolithic electronic components correspond to devices that integrate multiple passive components into a single chip structure. Such an integrated passive component may provide a selected combination of resistors, capacitors, inductors and/or other passive components that are formed in a multilayered configuration and packaged as a monolithic electronic device.

Selective terminations are often required to form electrical connections for various monolithic electronic components. Multiple terminations are needed to provide electrical connections to the different electronic components of an integrated monolithic device. Multiple terminations are also often used in conjunction with IDC's and other multilayer arrays in order to reduce undesirable inductance levels. One exemplary way that multiple terminations have been formed in multilayer components is by drilling vias through selected areas of a chip structure and filling the vias with conductive material such that an electrical connection is formed among selected electrode portions of the device.

Yet another way that terminations have been formed for multilayer electronic devices involves coating portions of termination lands with a solder stop material, thus forming a predefined area to which a solder ball or other solder preform may be applied.

Termination features for monolithic electronic components may also be designed such that small components are adapted for mounting to a relatively larger circuit board environment, such as in U.S. Patent No. 6,324,048 B1 (Liu) which is hereby incorporated by reference for all

purposes. This is especially true for capacitor devices, with which it is often preferred to have very small devices positioned in a very specific location on a printed circuit board or other substrate. Thus, unique arrangement of 5 internal and external component features may yield additional advancements in component configuration and termination.

While various aspects and alternative features are known in the field of capacitor formation and terminations 10 therefor, no one design has emerged that generally addresses all of the issues as discussed herein.

BRIEF SUMMARY OF THE INVENTION

The present subject matter recognizes and addresses various of the foregoing and other aspects of capacitor 15 formation, component termination, and related technology. Thus, broadly speaking, a principal object of the presently disclosed technology is improved formation of and 20 termination features for electronic components, and especially for multilayer capacitive devices.

Another principal object of the presently disclosed technology is to provide a multilayer capacitor with 25 internal electrode layers that are formed in an interdigitated fashion thus yielding an electrode configuration characterized by generally low equivalent series inductance (ESL). It has been found that the inductance of a capacitor is dominated by the inductance of the first layer, so in the exemplary configurations presented in accordance with the present subject matter, the overall inductance of the capacitor is 30 reduced by the very efficient structure as disclosed.

Yet another principal object of the present subject matter is to provide capacitor components that are

compatible with Ball Grid Array (BGA) mounting technology, thus providing multiple coplanar contacts on the underneath of a monolithic chip device.

A still further object of the present technology is to provide a multilayer device with a top cover layer having windows formed therein such that contacts can be directly plated to an internal electrode layer surface of the multilayer device. A transition layer may also be utilized such that all termination contacts can be made to a single layer within the multilayer device.

Yet another object of the present subject matter is to provide an improved multilayer capacitor and corresponding termination features that include an ability to put controlled equivalent series resistance (ESR) in a circuit environment with which the multilayer capacitor is used.

Additional objects and advantages of the invention are set forth in or will be apparent to those of ordinary skill in the art from the detailed description herein. Also, it should be further appreciated by those of ordinary skill in the art that modifications and variations to the specifically illustrated, referenced, and discussed features hereof may be practiced in various embodiments and uses of the disclosed technology without departing from the spirit and scope thereof, by virtue of present reference thereto. Such variations may include, but are not limited to, substitution of equivalent means and features, or materials for those shown, referenced, or discussed, and the functional, operational, or positional reversal of various parts, features, or the like.

Still further, it is to be understood that different embodiments, as well as different presently preferred embodiments, of the disclosed technology may include

various combinations or configurations of presently disclosed features or elements, or their equivalents (including combinations of features or configurations thereof not expressly shown in the figures or stated in the detailed description).

One exemplary embodiment of the presently disclosed technology corresponds to a multilayered assembly formed from a plurality of dielectric layers interleaved with a plurality of electrode layers. First and second transition layer electrode portions are provided on a top surface of the multilayered assembly, on top of which a cover layer is provided. The cover layer is formed to provide a plurality of openings therethrough to expose portions of the first and second transition layer electrodes. First and second peripheral terminations are formed along selected side surfaces of the capacitor's multilayered arrangement and electrically connect selected electrode layers to the respective first and second transition layer electrode portions.

In related embodiments, additional via terminations are formed in the openings defined by the cover layer, and solder balls may also be connected to the via terminations to facilitate component compatibility with ball grid array (BGA) mounting techniques. The via terminations, which may be multilayered terminations in some embodiments, can be formed by a variety of plating techniques.

The electrode layers and/or first and second transition layer electrode portions may be formed of a variety of materials, including ruthenium oxide, thereby introducing a predetermined amount of equivalent series resistance (ESR) into the multilayer capacitor.

Another exemplary embodiment of the present subject matter concerns a window via capacitor, which may correspond to a stacked multilayer configuration including at least one bottom layer, a plurality of first and second layers, a transition layer and a cover layer. An alternative variation of such window via capacitor comprises a stacked configuration of a bottom window layer, a bottom transition layer, a plurality of first and second layers, followed by a top window layer and a top cover layer.

More particularly, each first and second layer is preferably characterized by a sheet of dielectric material with a respective first or second electrode plate provided thereon. Each transition layer may also include a sheet of dielectric material on top of which transition layer electrode portions and/or anchor tabs may be provided. Adjacent first and second electrode plates form opposing active capacitor plates in the multilayer configuration. Portions of each first and second electrode plate extend to and are exposed on selected side portions of the periphery of the window via capacitor. Electrode and/or anchor tab portions of the transition layers are aligned in respective similar locations to the first and second electrode plates such that peripheral terminations can connect selected electrode portions of a first polarity together and selected portions of the opposing polarity together.

In some embodiments, the connection of peripheral terminations to the electrode portions of the transition layer collect the two opposing terminations onto a single planar surface. Window vias may then be formed through windows provided in the cover layer to effect low inductance electrical connection to the active components

of the window via capacitor. Other embodiments utilize windows in both the cover layer and the transition layer to form window via connections in two adjacent surfaces. Exemplary window vias may comprise single or multiple layers, such as successively plated layers of copper, nickel and tin, or successive layers of a metallic material, a resistor-polymeric material, and then a metallic material. Solder balls may also be applied to such window vias to yield a window via capacitor compatible with BGA mounting technology.

A still further exemplary embodiment of the present subject matter corresponds to a multilayer capacitor including a plurality of dielectric layers, respective pluralities of first and second electrode layers, at least one respective first and second via termination and at least one first and second respective peripheral termination. The respective pluralities of first and second electrode layers are interleaved with selected of the plurality of dielectric layers to form a multilayered assembly characterized by topmost and bottommost surfaces. The at least one first via termination is provided through the topmost layer of the multilayered assembly and is electrically connected to one of the first electrode layers, while the at least one second via termination is provided through the topmost layer of the multilayered assembly and is electrically connected to one of the second electrode layers. The at least one first peripheral termination is provided along selected side surfaces of the assembly and electrically connects the plurality of first electrode layers; similarly, the at least one second peripheral termination is provided along selected sides of

the assembly and electrically connects the plurality of second electrode layers.

Additional embodiments of the present subject matter, not necessarily expressed in this summarized section, may 5 include and incorporate various combinations of aspects of features or parts referenced in the summarized objectives above, and/or features or parts as otherwise discussed in this application.

Those of ordinary skill in the art will better 10 appreciate the features and aspects of such embodiments, and others, upon review of the remainder of the specification.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

A full and enabling description of the present subject 15 matter, including the best mode thereof, directed to one of ordinary skill in the art, is set forth in the specification, which makes reference to the appended figures, in which:

Figures 1A through 1E respectively illustrate 20 generally top views of exemplary successive layers for utilization in a first exemplary window via capacitor embodiment in accordance with the present subject matter;

Figure 2A provides a generally side exploded view with 25 slight top perspective of a first variation of a first exemplary window via capacitor embodiment with layers such as those illustrated in Figures 1A through 1E respectively;

Figure 2B provides a generally side exploded view with 30 slight top perspective of a second variation of a first exemplary window via capacitor embodiment with layers such as those illustrated in Figures 1A through 1E respectively;

Figure 3 provides a generally side view with slight top perspective of a first exemplary window via capacitor embodiment in accordance with the present subject matter;

Figures 4A and 4B provide a generally side cross-

5 sectional views of respective first and second variations of a first exemplary window via capacitor embodiment, such as taken along cut line A-A of Figure 3, with the further addition of specific exemplary mounting features (in this instance, solder balls) in accordance with the present
10 subject matter;

Figure 5 provides an enlarged, generally side cross-sectional view of an exemplary window via in accordance with an exemplary window via capacitor of the present
subject matter;

15 Figures 6A through 6E respectively illustrate generally top views of exemplary successive layers for utilization in a second exemplary window via capacitor embodiment in accordance with the present subject matter;

20 Figure 7A provides a generally side view with slight top perspective of a second exemplary window via capacitor embodiment in accordance with the present subject matter;

25 Figure 7B provides a generally side view of a second exemplary window via capacitor embodiment with specific exemplary mounting features (in this instance, solder balls) in accordance with the present subject matter;

Figures 8A through 8E respectively illustrate generally top views of exemplary successive layers for utilization in a third exemplary window via capacitor embodiment in accordance with the present subject matter;

30 Figure 9A provides a generally side view of a third exemplary window via capacitor embodiment in accordance with the present subject matter; and

Figure 9B provides a generally side exploded view with slight top perspective of a third exemplary window via capacitor embodiment with specific exemplary mounting features (in this instance, solder balls) in accordance with the present subject matter.

5 Repeat use of reference characters throughout the present specification and appended drawings is intended to represent same or analogous features or elements of the present technology.

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DETAILED DESCRIPTION OF THE EMBODIMENTS

As referenced in the Brief Summary of the Invention section, the present subject matter is directed towards improved component formation and termination features for multilayer capacitors and other electronic components.

15 The subject "window via capacitors" utilize at least one cover layer with window-like openings that expose portions of internal electrode layers or optional transition layers such that electrical contacts can be directly plated to such exposed areas. It is desired to form a plurality of 20 co-planar terminations such that solder balls may be applied in accordance with BGA mounting techniques.

25 Several exemplary embodiments of the subject window via capacitor technology are presented herein to relay significant aspects of the present subject matter. Figures 1A through 5, respectively, illustrate aspects of a first exemplary window via capacitor embodiment of the present technology, including first and second variations thereof. Figures 6A through 7, respectively, depict a second 30 exemplary window via capacitor embodiment of the present technology as well as related aspects thereof. A third exemplary embodiment of the present subject matter is

presented with respect to Figures 8A through 9B, respectively.

It should be noted that each of the exemplary embodiments as presented herein should not insinuate limitations of the disclosed technology. Features 5 illustrated or described as part of one embodiment can be used in combination with another embodiment to yield further embodiments. Additionally, certain features may be interchanged with similar devices or features not mentioned 10 yet which perform the same, similar or equivalent function.

Furthermore, some of the capacitors are shown with terminals only on a selected top or bottom surface of the multilayer component. Some applications may prefer or even require that the component be symmetrical with respect to 15 top and bottom surfaces, so that they can be assembled using automated equipment or to permit electrical feed-through connections. In such cases, the construction described forming selected top surfaces can also be used for selected bottom surfaces, as represented in exemplary 20 embodiment 40b of Figures 2B and 4B.

Reference will now be made in detail to the presently preferred embodiments of the disclosed technology. Referring to the drawings, Figures 1A through 1E illustrate generally top views of exemplary successive layers for 25 utilization in a first exemplary window via capacitor 40 (such as represented in the exploded views of Figure 2A and 2B.) A first layer 10 as represented in Figure 1A comprises a sheet of dielectric material 12a which is partially covered by a first electrode plate 14. Electrode 30 plate 14 may be formed such that a portion of the electrode plate extends to and along at least one entire edge 16 of dielectric sheet 12b. When a plurality of layers are

successively stacked on top of one another, portions of the electrode plates will thus be exposed at selected side portions of the multilayer device.

A second layer 18 that may be utilized in forming a first exemplary window via capacitor is illustrated in Figure 1B, and is similar to the first layer 10 of Figure 1A. Second layer 18 preferably comprises a sheet of dielectric material 12b which is partially covered by a second electrode plate 20. Electrode plate 20 may be formed such that a portion of the electrode plate extends to and along at least one entire edge 22 of dielectric sheet 12b. The portion of electrode plate 20 exposed at edge 22 and any adjacent exposed portions preferably opposes the portion of electrode plate 10 formed by edge 16. As will be further discussed with reference to Figures 2A and 2B, first layer 10 and second layer 18 can be provided adjacent to one another in a layered stack such that electrode plates 14 and 20 respectively form the opposing active plates of a parallel-plate capacitor.

A transition layer is also preferably employed in a first exemplary embodiment of the subject window via capacitor technology. Two exemplary transition layers 24a and 24b are respectively illustrated in Figures 1C and 1D. Either transition layer embodiment may be utilized in the window via capacitor embodiments in accordance with the present subject matter. As such, discussion herein with regards to a transition layer 24 concerns both such exemplary transition layers 24a and 24b. Also, when the figures and/or discussed embodiments include a transition layer 24, either exemplary transition layer 24a or 24b or some other variation thereof may be utilized. The same situation holds for reference number 26, corresponding

to portions 26a and/or 26b, and reference number 28, corresponding to portions 28a and/or 28b.

Transition layers 24a and 24b, top views of which are respectively depicted in Figures 1C and 1D, comprise a sheet of dielectric material 12c on top of which is provided a first transition layer electrode portion 26 and a second transition layer electrode portion 28. First transition layer electrode portion 26 preferably extends to the same selected edge 16 to which electrode plate 14 of Figure 1A extends, and transition layer electrode portion 28 preferably extends to the same selected edge 22 to which electrode plate 20 of Figure 1B extends. Transition layer electrode portions may be generally rectangular in shape such as portions 26a and 28a of Figure 1C, or may be have a generally U-shaped configuration, such as portions 26b and 28b of Figure 1D.

It should be appreciated that the formation of the electrode plates 14 and 20 and the transition layer 24 with electrode portions 26 and 28, as well as the location of exposed portions thereof, may be along one or many edges. Modifications to the disclosed electrode plates and portions is within the spirit and scope of the present technology as long as a selected plurality of the electrode portions remain exposed at a first aligned peripheral location and an additional selected plurality of the electrode portions remain exposed at least one other different peripheral location.

Figure 1D displays an exemplary cover layer 30 for use in a first exemplary window via capacitor embodiment of the present subject matter. Cover layer 30 comprises a sheet 12d of dielectric material that is formed to define a first plurality of windows 32a and 32b (hereafter collectively

referred to as 32) as well as a second plurality of windows 34a and 34b (hereafter collectively referred to as 34.) In some embodiments of the present technology, cover layer 30 is characterized by an exemplary thickness of about one mil. Such windows 32 and 34 are utilized to form window via terminations in accordance with the present subject matter, as will be further appreciated with respect to the remaining discussion.

Dielectric sheets 12a-12d, may respectively comprise any type of semiconductive or ceramic material suitable for use in capacitive or other types of electronic components, including barium titanate, zinc oxide, alumina with low-fire glass, or other suitable ceramic or glass-bonded materials. In some embodiments of the present technology, dielectric sheets 12a-12d may have thickness in a range of about five to about twenty-five microns. Electrode plates 14 and 20 as well as transition layer electrode portions 26 and 28 may comprise any conductive material suitable for use as an electrode plate, such as platinum, gold, nickel, niobium, palladium, ruthenium, iridium, ruthenium oxide, iridium oxide, other suitable conductive materials, or a combination or alloy of selected of the above-referenced substances. By employing a material with resistive properties, such as ruthenium oxide, in electrode plates and/or electrode portions of the present technology, then controlled equivalent series resistance (ESR) may be introduced into the subject window via capacitors.

The layers illustrated in Figures 1A through 1E respectively, may be combined together to form a first exemplary window via capacitor embodiment of the subject technology (variations of which are respectively illustrated in Figures 2A and 2B.) Such window via

capacitor is a multilayer structure discussed herein with regards to layers being successively stacked in a particular order and/or relationship from bottom to top. It should be appreciated that such bottom and top reference 5 is used merely for the sake of convenience. The bottom layers may actually be the top layers when such capacitor is mounted to a circuit board.

Referring to the exemplary window via capacitor 40a of Figure 2A, the bottom layers may comprise at least one (two 10 are shown in Figure 2A) sheet 42 of dielectric material. Sheets 42 may be similar to the dielectric sheets 12a-12c, and may comprise similarly selected materials. Such bottom 15 layers are provided to add support to the multilayered structure of first exemplary embodiment 40a and protection for the other layers and active components thereof. After providing bottom layers 42, at least one first layer 10 and at least one second layer 18 are provided. Such first and 20 second layers are preferably provided in an alternating fashion and in corresponding pairs such that the electrode plates of a given first layer 10 and an adjacent second layer 18 form opposing capacitor plates. It should be appreciated that three first layers 10 and three second 25 layers 18 are illustrated in Figure 2A for exemplary purposes only and that any number of first and second layers 10 and 18 may be provided in accordance with the present technology. After providing first and second layers 10 and 18, a transition layer 24 and a cover layer 30 are respectively added to the stacked configuration of embodiment 40a.

Figure 2B illustrates another exemplary window via 30 capacitor embodiment 40b, which may be similar to Figure 2A except for the bottommost layers of the device. As

previously mentioned, some applications require that a component be symmetrical with respect to top and bottom surfaces. As such, the bottom layers of Figure 2B preferably comprise a transition layer 24 and cover layer 30 (similar to the top two layers.) It should be noted that for symmetry, the bottom transition layer 24 is stacked in a reverse orientation to the top transition layer 24. In this way, the bottom layers are actually the same as the top layers, but reversed, so that after termination it does not matter which side the user 10 positions down for mounting.

Once the selected layers for a window via capacitor are stacked and fired together, terminations to the internal electrode plates and transition layer electrode portions may be effected. First capacitor embodiments 40a and 40b (collectively referred to in Figures 3 and 5 as embodiment 40) may be terminated on the ends as shown in Figure 3 to connect all electrodes of a first polarity together and similarly to connect all electrodes of the opposing polarity together. Peripheral termination 44 is preferably connected to the exposed portions of electrode plates 14 and first transition layer electrode portion(s) 26. Such first peripheral termination 44 extends across the entire side 16 of the capacitor 40 and may wrap around 20 to selected parts of the adjacent sides of the device. Peripheral termination 46 is preferably connected to the exposed portions of electrode plates 20 and second transition layer portion(s) 28. Such second peripheral 25 termination 46 extends across the entire side 22 of the capacitor 40 and wraps around to selected parts of the adjacent sides of the device.

Peripheral terminations 44 and 46 may be formed by application of a "thick-film" conductive termination material, such as silver or copper paste. Peripheral terminations 44 and 46 may alternatively be formed by effecting deposition of a conductive material to selected exposed electrode portions and ultimately forming "plated terminations." Such plated terminations may be formed by electroplating or electrochemical deposition, wherein capacitor 40 with exposed electrode portions is subjected to a plating solution such as electrolytic nickel or electrolytic tin characterized by an electrical bias. The capacitor itself is then biased to a polarity opposite that of the plating solution, and conductive elements in the plating solution are attracted to selected of the exposed electrode portions of the capacitor. Such a plating technique with no polar biasing is referred to as electroless plating, and can be employed in conjunction with electroless plating solutions such as nickel or copper ionic solution.

In accordance with electrochemical deposition and electroless plating techniques, capacitor 40 is preferably submersed in an appropriate plating solution for a particular amount of time. With certain embodiments of the present subject matter, no longer than fifteen minutes is required for enough plating material to deposit at selected exposed electrode portions along a window via capacitor such that buildup is enough to spread the plating material to create a continuous connection among selected adjacent exposed electrode portions.

Another technique that may be utilized in accordance with the formation of plated terminations involves magnetic attraction of plating material. For instance, nickel

particles suspended in a bath solution can be attracted to selected similarly conductive exposed electrode portions of a capacitor by taking advantage of the magnetic properties of nickel. Other materials with similar magnetic properties may be employed in the formation of plated terminations.

A still further technique regarding the application of plated termination material to selected exposed electrode portions of a window via capacitor involves the principles of electrophoretics or electrostatics. In accordance with such exemplary technology, a bath solution contains electrostatically charged particles. A window via capacitor with exposed electrode portions may then be biased with an opposite charge and subjected to the bath solution such that the charged particles are deposited at select locations on the component. This technique is particularly useful in the application of glass and other semiconductive or nonconductive materials. Once such materials are deposited, it is possible to thereafter convert the deposited materials to conductive materials by intermediate application of excessive heat to the component.

One particular methodology for forming plated terminations in accordance with the disclosed technology relates to a combination of the above-referenced plating application techniques. A window via capacitor may first be submersed in an electroless plating solution, such as copper ionic solution, to deposit an initial layer of copper over selected exposed electrode portions. The plating technique may then be switched to an electrochemical plating system which allows for a faster

buildup of copper on the selected portions of such component.

In accordance with the different available techniques for plating material to selected exposed electrode portions 5 of a window via capacitor in accordance with the present technology, different types of materials may be used to create the plated terminations. For instance, metallic conductors such as nickel, copper, tin, etc. may be utilized as well as suitable resistive conductors or semi- 10 conductive materials (such as are provided in accordance with varistor technology), and/or combinations of selected of these different types of materials.

Plated terminations in accordance with the present subject matter are guided by the position of exposed 15 electrode portions: Such phenomena may be referred to as "self-determining" since the formation of plated terminations is determined by the configuration of exposed metallization at selected peripheral locations on the window via capacitor. Further assurance of complete 20 plating coverage and bonding of the plated materials may be achieved by including resistance-reducing additives in the plating solution(s). A still further mechanism for enhancing the adhesion of metallic deposit that forms the plated terminations is to thereafter heat the component in 25 accordance with such technologies as baking, laser subjection, UV exposure, microwave exposure, arc welding, etc.

The connection of peripheral terminations 44 and 46 to electrode portions of a transition layer collect the two 30 opposing terminations onto a single planar surface.

Electrical connection to all active portions of capacitor 40 can thus be effected through connection to the

respective electrode portions of one or more transition layer(s). Referring to Figures 2A and 2B, the first plurality of windows 32 provides exposed access to the first transition layer electrode portion(s) 26 and the second plurality of windows 34 provides exposed access to the second transition layer electrode portion(s) 28. Although only two windows are illustrated in each of respective pluralities 32 and 34, it should be appreciated that a greater or fewer number of windows may be provided to expose the electrode portions of transition layer 24. The windows may also be relocated to suit a particular set of contacts on the substrate to which the part will be mounted.

Windows 32 and 34 defined in cover layer 30 may also be thought of as ceramic solder dams in which window vias 48 may be formed. A detailed view of a portion of first exemplary capacitor 40 is represented in Figure 5, which illustrates the window 32a formed in cover layer 30. It should be appreciated that the following discussion with respect to window 32a may be equally applicable to other windows and window vias of the present technology. An exemplary thickness 50 for cover layer 30 is about thirty-five microns, while an exemplary width 52 for window 32a is about five mils (one-hundred-twenty-seven microns.)

Still referring to Figure 5, a window via may be formed in window 32a (and in other windows) to provide termination to the exposed portion of electrode portion 26 of transition layer 24. Window via 48 may comprise a single termination layer or multiple termination layers, each of which may be characterized by a variety of material compositions and/or specified thickness. One particular example of a window via 48 includes a first plated layer 54

of copper, a second plated layer 56 of nickel and a third plated layer 58 of tin. Another example of a window via 48 includes a first plated metallic layer, a second plated layer of resistor-polymeric material, and a third additional metallic layer, for example made of tin or copper. Yet another example of a window via 48 includes a first plated metallic layer and a second plated layer of a resistive alloy.

Such plated multilayer window vias may be formed in accordance with the "plated termination" technology previously addressed with respect to first and second peripheral terminations 44 and 46. It should be appreciated that any variety of materials may be employed in the formation of window vias 48, while still remaining within the spirit and scope of the present subject matter. It should be further appreciated that aspects of the specific exemplary multi-layered window via configurations and materials used therein, as discussed in the preceding paragraph, may also be utilized in some embodiments of peripheral terminations 44 and 46.

Figures 4A and 4B provide cross-sectional views of respective variations of first exemplary window via capacitor 40 as taken along cut line A-A in Figure 3, with the addition of exemplary window vias as presented in Figure 5 and with the further addition of solder balls in accordance with the present technology. Figure 4a illustrates additional aspects of the layered configuration presented with respect to embodiment 40a of Figure 2A, while Figure 4b illustrates additional aspects of the layered configuration presented with respect to embodiment 40b of Figure 2B. Solder balls 60, for example a C4 solder bump, may be placed on the respective contact areas formed

by plated tin layers 58 (or other upper window via surfaces) formed in cover layers 30. Solder balls 60 may then be reflowed to give a Ball Grid Array (BGA) contact formation.

5 Figures 6A through 6E respectively illustrate generally top views of exemplary successive layers for utilization in a second exemplary window via capacitor 140, such as shown in Figures 7A and 7B. Since elements presented with respect to such second exemplary embodiment
10 140 are similar to elements presented with respect to the first exemplary embodiment 40, similar reference numbers but in a "100" series are used to indicate such similar elements. For instance, an element in first embodiment 40 having reference number 20 would have a reference number
15 120 to depict a similar element in such different embodiment. Aspects of the present subject matter addressed with respect to first exemplary embodiment 40 may be equally applicable to second exemplary embodiment 140.

As such, Figure 6A illustrates an exemplary bottom layer 142, which comprises a sheet of dielectric material. Figure 6B illustrates an exemplary first layer 110 corresponding to a sheet 112a of dielectric material partially covered by a first electrode plate 114. Portions of first electrode plate 114 preferably extend to selected edges of dielectric sheet 112a. Electrode plate 114 may comprise a main portion with electrode tabs 115 that extend from the main portion to selected edges of dielectric sheet 112a. Figure 6C illustrates an exemplary second layer 118 comprising a sheet 112b of dielectric material partially
25 covered by a second electrode plate 120. Portions of second electrode plate 120 preferably extend to selected edges of dielectric sheet 112b at differently aligned
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locations than where portions of first electrode plate 114 extends. Electrode plate 120 may comprise a main portion with electrode tabs 119 that extend from the main portion to selected edges of dielectric sheet 112b.

- 5 Still referring to a second exemplary window via capacitor embodiment 140 of the present subject matter, Figure 6D illustrates an exemplary transition layer 124 which comprises a sheet 112c of dielectric material partially covered by transition layer electrode portions.
- 10 A first transition layer electrode portion 126 and plurality of first anchor tab portions 127 are preferably aligned in the same location as portions of first electrode plate 114 and tabs 115 thereof. By exposing such first electrode plate 114 and tabs 115 at the same location along edges of the first layer 110 as where the first transition
- 15 layer electrode portion 126 and first plurality of anchor tabs 127 are exposed along edges of transition layer 124, peripheral terminations can be used to connect a plurality of such layers together. Similarly, a second transition
- 20 layer electrode portion 128 and plurality of second anchor tab portions 129 are preferably aligned in the same location as portions of second electrode plate 120 and tabs 119 thereof. By exposing such second electrode plate 120 and tabs 119 at the same location along edges of the second
- 25 layer 118 as where the second transition layer electrode portion 128 and second plurality of anchor tabs 129 are exposed along edges of transition layer 124, peripheral terminations can be used to connect a plurality of these such layers together. In some embodiments of the present
- 30 technology, anchor tabs 127 and 129 may respectively be about 10 mils long and about 15 mils wide.

Figure 6E provides an exemplary cover layer 130 for use in second exemplary window via capacitor embodiment 140 of the present subject matter. Cover layer 130 comprises a sheet 112d of dielectric material that is formed to define 5 a first plurality of windows 132a through 132d respectively (hereafter collectively referred to as 132) as well as a second plurality of windows 134a through 134d respectively (hereafter collectively referred to as 134.) The first plurality of windows 132 provides exposed access to the 10 first transition layer electrode portion 126 and plurality of first anchor tabs 127. The second plurality of windows 134 provides exposed access to the second transition layer electrode portion 128 and plurality of second anchor tabs 129. Although only four windows are illustrated in the 15 respective pluralities 132 and 134, it should be appreciated that a greater or fewer number of windows may be provided to expose the electrode portions of transition layer 124.

The respective layers illustrated in Figures 6A through 6E are to be layered in a determined stacked configuration, just as the circumstances for the exploded stacks depicted in Figures 2A and 2B. At least one bottom 20 layer 142, a plurality of alternating first layers 110 and second layers 118, a transition layer 124 and a cover layer 130 may be stacked together to form second exemplary 25 embodiment 140 of Figures 7A and 7B. The electrode plates 114 and 120 of each adjacent pair of layers 110 and 118 form opposing active capacitor plates. Instead of bottom layers 142, another transition layer 124 and cover layer 30 130 may be utilized to form a more symmetrical component. After forming and firing such a stacked configuration, terminations to the internal electrode plates and

transition layer electrode portions and anchor tabs may be effected.

Second capacitor embodiment 140 may be terminated on selected sides of the multilayer device as shown in Figures 5 7A and 7B to connect all electrodes of a first polarity together and similarly to connect all electrodes of the opposing polarity together. Peripheral termination 144 preferably connects selected exposed portions of electrode plates 114 to first transition layer electrode portion 126. 10 Peripheral terminations 145a and 145b, as well as two other peripheral terminations on the opposing side of capacitor 140 (not shown in Figure 7B), preferably connect additional exposed portions of electrode plates 114 (namely electrode tabs 115) to transition layer anchor tabs 127. Peripheral 15 termination 146 preferably connects selected exposed portions of electrode plates 120 to second transition layer electrode portion 128. Peripheral terminations 147a and 147b, as well as two other peripheral terminations on the opposing side of capacitor 140 (not shown in Figure 7B), 20 preferably connect additional exposed portions of electrode plates 120 (namely electrode tabs 119) to transition layer anchor tabs 129. Peripheral terminations 144 and 146 may be used for electrical test, thus simplifying the test process. Further, they can also provide simple contact to 25 the exposed electrode surfaces in the windows, so they can be electroplated.

Referring still to Figures 7A and 7B, the connection of peripheral terminations 144, 146, 145a, 145b, 147a and 147b to the electrode portions of transition layer 124 30 collect the two opposing terminations onto a single planar surface. Electrical connection to all active portions of capacitor 140 can thus be effected through connection to

the respective electrode portions of transition layer 124. Such electrical connections may be effected by window vias 148 formed in windows 132 and 134. As previously discussed, window vias formed in accordance with the 5 present technology may be formed with any combination of materials and with any specified thickness. Window vias 148 may generally correspond to a solderable round pad to which solder balls 160 may be placed and reflowed. Solder balls 160 thus provide electrical connection to all active 10 portions of window via capacitor 140 while terminating capacitor 140 with BGA mounting features.

Exemplary dimensions for the second exemplary window via capacitor embodiment 140 of the present technology are represented in Figure 7A. In some embodiments, capacitor 15 140 may be characterized by a thickness 170 of about forty mils, a width 172 of about eighty mils and a length 174 of about one-hundred-twenty mils. An exemplary width pitch 176 between adjacent window vias 148 may be about sixty mils and an exemplary length pitch 178 between adjacent 20 window vias 148 may be about thirty mils.

Figures 8A through 8E respectively illustrate generally top views of exemplary successive layers for utilization in a third exemplary window via capacitor 240, such as shown in Figures 9A and 9B. Since elements 25 presented with respect to such third exemplary embodiment 240 are similar to elements presented with respect to the first exemplary embodiment 40 and second exemplary embodiment 140, similar reference numbers but in a "200" series are used to indicate such similar elements. For 30 instance, an element in first embodiment 40 having reference number 20 would have a reference number 220 to depict a similar element in such third exemplary

embodiment. Aspects of the present subject matter addressed with respect to first exemplary embodiment 40 and/or with respect to second exemplary embodiment 140 may be equally applicable to third exemplary embodiment 240.

As such, Figure 8A illustrates an exemplary bottom layer 242, which comprises a sheet of dielectric material. Figure 8B illustrates an exemplary first layer 210 corresponding to a sheet 212a of dielectric material partially covered by a first electrode plate 214. Portions of first electrode plate 214 preferably extend to selected edges of dielectric sheet 212a. Electrode plate 214 may comprise a main portion with electrode tabs 215 that extend from the main portion to selected edges of dielectric sheet 212a. Figure 8C illustrates an exemplary second layer 218 comprising a sheet 212b of dielectric material partially covered by a second electrode plate 220. Portions of second electrode plate 220 preferably extend to selected edges of dielectric sheet 212b at differently aligned locations than where portions of first electrode plate 214 extends. Electrode plate 220 may comprise a main portion with electrode tabs 219 that extend from the main portion to selected edges of dielectric sheet 212b.

Still referring to a third exemplary window via capacitor embodiment of the present subject matter, Figure 8D illustrates an exemplary transition layer 224 which comprises a sheet 212c of dielectric material partially covered by transition layer electrode portions. A first transition layer electrode portion 226 may be generally similar in shape to the first electrode plate 214. By exposing each first electrode plate 214 and tabs 215 at the same location along edges of the first layer 210 as where the first transition layer electrode portion 226 are

exposed along edges of transition layer 224, peripheral terminations can be used to connect a plurality of such layers together.

With further reference to the exemplary transition
5 layer 224 of Figure 8D, the dielectric sheet 212c may be formed to define a plurality of transition layer windows 225 which may expose portions of an underlying electrode plate 220 of second layer 218.

Figure 8E provides an exemplary cover layer 230 for
10 use in second exemplary window via capacitor embodiment 240 of the present subject matter. Cover layer 230 comprises a sheet 212d of dielectric material that is formed to define a first plurality of windows 232a through 232d respectively (hereafter collectively referred to as 232) as well as a
15 second plurality of windows 234a through 234d respectively (hereafter collectively referred to as 234.) The first plurality of windows 232 provides exposed access to the first transition layer electrode portion 226. The second plurality of windows 234 in conjunction with windows 225 of
20 transition layer 224 provide exposed access to the top second electrode plate 220 of top second layer 218.
Although only four windows are illustrated in the respective pluralities 225, 232 and 234, it should be appreciated that a greater or fewer number of windows may
25 be provided to expose the electrode portions of transition layer 224 and second layer 218. Further, these windows can be adjusted to fit the particular pattern of the substrate to which the part will be mounted.

The respective layers illustrated in Figures 8A
30 through 8E are to be layered in a determined stacked configuration, an example of which is depicted in Figures 9A and 9B. At least one bottom layer 242, a plurality of

alternating first layers 210 and second layers 218, a transition layer 224 and a cover layer 230 may be stacked together to form third exemplary embodiment 240 of Figures 9A and 9B. The electrode plates 214 and 220 of each adjacent pair of layers 210 and 218 form opposing active capacitor plates. Such first and second layers are preferably arranged with an equal number of each and such that a second layer 218 is provided on top, such that subsequent provision of a transition layer 224 and a cover layer 230 exposes appropriate electrode portions for making electrical connection thereto.

Although not shown, it should be appreciated that instead of a bottom layer 242, another transition layer 224 and cover layer 230 may be utilized to form a more symmetrical component (such as in exemplary embodiment 40b), than that depicted in Figure 9B.

After forming and firing a stacked configuration of the layers depicted in Figures 8A through 8E respectively, terminations to the internal electrode plates and transition layer electrode portion may be effected. Third capacitor embodiment 240 may be terminated on selected sides of the multilayer device with peripheral terminations (not shown) that connect all electrodes of a first polarity together and similarly connect all electrodes of the opposing polarity together. Window vias may then provide additional termination features for capacitor 240.

Although selected such window vias in accordance with third exemplary embodiment 240 may extend through windows in two layers, the resultant capacitor 240 is characterized by an relatively low inductance terminations and lower overall ESL.

Referring still to Figures 9A and 9B, electrical connection to all active portions of capacitor 240 can thus be effected through connection to the respective electrode portions of transition layer 224 and top second layer 218. Such electrical connections may be effected by window vias 248a and 248b. Window vias 248a preferably extend through windows 232 to transition layer electrode portion 226, while window vias 248b preferably extend through windows 234 and underlying windows 225 to top second electrode plate 220. As previously discussed, window vias formed in accordance with the present technology may be formed with any combination of materials and with any specified thickness. As depicted in Figure 9B, solder balls 260 may then be reflowed to selected ends of vias 248a and 248b thus providing electrical connection to all active portions of window via capacitor 240 while terminating capacitor 240 with BGA mounting features.

While the present subject matter has been described in detail with respect to specific embodiments thereof, it will be appreciated that those skilled in the art, upon attaining an understanding of the foregoing may readily adapt the present technology for alterations to, variations of, and equivalents to such embodiments. Accordingly, the scope of the present disclosure is by way of example rather than by way of limitation, and the subject disclosure does not preclude inclusion of such modifications, variations, and/or additions to the present subject matter as would be readily apparent to one of ordinary skill in the art.